REMARKS/ARGUMENTS

This is in response to an Office action dated 10/13/2005.

Status
Claims 1-18 are pending
Claims 1-18 are rejected
Claim 4 is objected to

Claim Objections

Claims 4 and 5 are objected to because claim 4 is a duplicate of claim 5.

Claim 5 is amended, and is now similar to claims 13 and 18.

Rejection(s) under 35 USC 103

Claims 1-5, 7-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Pat. 2004/0214446) in view of Stojakovic et al (US Pat. 2005/0051820).

The present claim generally requires a method of forming an oxidized tantalum nitride hard mask for dual damascene processing, the method comprising providing a semiconductor wafer, the wafer comprising: a base dielectric layer, a cap layer overlying the base dielectric layer, a dielectric layer overlying the cap layer, one or more hard mask layer overlying the dielectric layer and a tantalum nitride layer overlying the hard mask layers, subjecting the tantalum nitride layer to an oxidation process to convert tantalum nitride layer to oxidized tantalum nitride (TaO_xN_x).

Regarding claim 1, Figure 1 of Kim et al. discloses a semiconductor wafer comprising a dielectric layer 105, a cap layer 110, overlying the base dielectric a dielectric layer 112, overlying the cap layer a hard mask layer 114, overlying the dielectric layer and forming trench 116 (See page. 5, paragraph [0060-621]), a tantalum nitride layer 324 overlying the hard mask layer (See page. 8, paragraph [0086]).

Kim et al discloses all of the claimed features as stated above except for forming a tantalum nitride layer overlying the hard mask layers and subjecting the tantalum nitride layer to an oxidation process to convert tantalum nitride layer to oxidized tantalum nitride (TaO_xN_x).

Stojakovic et al. discloses exposing a multiple hard mask layer such as a tantalum nitride layer to an oxidation process to convert the tantalum nitride layer to oxidized tantalum nitride layer (See page. 1 , paragraph [0007]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to

use the oxidation process for converting tantalum nitride layer to oxidize the tantalum nitride of Stojakovic et al., in the stack layers of Kim et al. for it's known benefit of providing a hard mask structure for etching. As both reference disclose hard mask structures, and each disclose the use of tantalum nitride or oxidized tantalum nitride as a hard mask, the substitution of one hard mask Layer for another would have been prima fade obviousness. The use of a known hard mask oxidized tantalum nitride, for its known purpose is prima fadc obviousness.

Regarding claim 2, Kim et al. discloses a metal conductor such as copper is planarized using chemical mechanical polishing (Page 6, 7 paragraph [0074]). Kim et al. also discloses a conductive material such as copper has a low resistivity, which is a material of choice for sub-quarter-micron interconnect (See page 1 , paragraph [0007]).

Regarding claims 3, 10 and 15 Kim et al. discloses a single dielectric material such as silicon oxycarbide 112 is deposited on layer 110 (page 5, paragraph [0061]).

Regarding claims 5, 11 and 16, Figure 1 of Kim et al discloses the dielectric layers 110, 112 and 114 "stack-up", where the hybrid dielectric known as a multiple layer for processing

Regarding claim 7, Kim et al. is relied upon as discussed above and disclose all of the claimed features as stated above except for the creating a patterned photoresist layer and etching the tantalum nitride layer prior to oxidation.

Stojakovic et al. discloses patterning a photoresist layer and etching the tantalum nitride layer prior to oxidation (See page. 2 paragraph [0011]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to pattern a photoresist layer and etch a tantalum nitride hard mask layer prior to oxidation, in light of the disclosure of Stojakovic et al. which teaches patterning and etching a tantalum nitride hard mask prior to oxidation. It would have been obvious to one of ordinary skill in the art to pattern and etch the hard mask of Kim et al. prior to the oxidation as discloses by Stojakovic et al. for it's known benefit of patterning and etching a hard mask. The transposition of process steps would be obvious in light of the disclosure of Stojakovic et al.

Regarding claim 8, Kim et al. discloses all of the claimed features as stated above except for creating a pattern of photoresist layer and etching the oxidized tantalum nitride layer after the oxidation process.

Stojakovic et al. discloses a patterning a photoresist layer and etching the oxidized tantalum nitride layer after the oxidation process (See page. 2 paragraph [0013]).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to

pattern a photoresist layer and etch the oxidized tantalum nitride hard mask layer after the oxidation, in light of the disclosure of Stojakovic et al. which teaches patterning and etching the oxidized tantalum nitride hard mask layer after the oxidation process. It would have been obvious to one of ordinary skill in the art to pattern and etch the hard mask of Kim et al. after the oxidation as discloses by Stojakovic et at, for it's known benefit of patterning and etching a hard mask. The transposition of process steps would be obvious in light of the disclosure of Stojakovic et al.

Regarding claim 9, Figure 3D of Kim et al. discloses a dual-damascene method of processing a semiconductor wafer comprising a base dielectric layer 305 having circuit elements and planarized flush with the surface thereof to which a subsequent electrical connection is to be made (See page. 8 paragraph [0087]), forming a cap layer 310 over the base dielectric layer 305 and circuit elements, forming a dielectric layer 312 over the cap layer 310 and forming a first hard mask layer (HM1) 322 over the dielectric layer 312 and forming a tantalum nitride layer 324 over the hard mask layer (See page. 7 paragraph [0078, 79, 83 and 86]) and lithographically etching the tantalum nitride layer to form trench opening (See figure. 1).

Kim et al. discloses all of the claimed features as stated above except for forming a second hard mask layer (HM2) over the first hard mask layer and etched tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer.

Stojakovic et al. discloses a method of forming a second hard mask layer (HM2) over the first hard mask layer and forming a tantalum nitride layer over the second hard mask layer and etched tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer. Stojakovic et al discloses a hard mask may comprises one or more layers made from titanium, tantalum, tantalum nitride, titanium nitride, titanium oxide, tantalum oxide, or any combination thereof, for example. As one example, the hard mask may include a tantalum nitride layer, a titanium layer over the tantalum nitride layer, and a titanium nitride layer over the titanium layer. (See page. 1 paragraph [0007]). Also see figure. 5

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the first and second hard mask layer and forming tantalum nitride layer over the second hard mask layer and etch tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer of Stojakovic et al. in the process of Kim et at. for it's known benefit of forming a hard mask layer and etching a tantalum nitride to an oxidation process to form an oxidized tantalum nitride layer. As both reference disclose hard mask structures, and each disclose the use of tantalum nitride or oxidized tantalum nitride as a hard mask, the substitution of one hard mask layer for another would have been prima facie obviousness. The use of a known hard mask oxidized tantalum nitride for its known purpose is prima fade obviousness. The use of multiple hard mask layer is obvious in light of Stojakovic et at. which teaches to use multiple hard mask layer.

Regarding claim 14, Figure 3D of Kim et at. discloses a dual-damascene method of processing a semiconductor wafer comprising a base dielectric layer 305 having circuit elements and planarized flush with the surface thereof to which a subsequent electrical connection is to be made (See page 8 paragraph (0087]), forming a cap layer 310 over the base dielectric layer 305 and circuit elements, forming a dielectric layer 31 2 over the cap layer 31 0 and forming a first hard mask layer (HMI) 322 over the dielectric layer 312 and lithographically etching the oxidized tantalum nitride layer to form trench opening (See figure 1).

Kim et at. discloses all of the claimed features as stated above except for forming a second hard mask layer (HM2) over the first hard mask layer and subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer.

Stojakovic et at. discloses a method of forming a second hard mask layer (HM2) over the first hard mask layer and forming a tantalum nitride layer over the second hard mask layer and subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer. Stojakovic et at, also discloses a hard mask may comprises one or more layers made from titanium, tantalum, tantalum nitride, titanium nitride, titanium oxide, tantalum oxide, or any combination thereof, for example. As one example, the hard mask may include a tantalum nitride layer, a titanium layer over the tantalum nitride layer, and a titanium nitride layer over the titanium layer. (See page. 1 paragraph [0007]). Also see figure. 5

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the first and second hard mask layers and forming a tantalum nitride layer over the second hard mask layer and subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer of Stojakovic et at. in the process of Kim et al. for it's known benefit of forming a hard mask layer and oxidizing tantalum nitride layer and etching the oxidized tantalum nitride layer to form trench. As both reference disclose hard mask structures, and each disclose the use of tantalum nitride or oxidized tantalum nitride as a hard mask, the substitution of one hard mask layer for another would have been prima fade obviousness. The use of a known hard mask oxidized tantalum nitride for its known purpose is prima fade obviousness. The use of multiple hard mask layers is obvious in light of Stojakovic et at., which teaches to use multiple hard mask layers.

Claims 6, 12, 13, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Pat. 2004/0214446) in view of Stojakovic et al (US Pat. 2005/0051820) further in view of Narwankar et at. (US Pat. 2003/0025146).

Regarding claim 6, 12, 13, 17 and 18, Kim et at. and Stojakovic et at. are relied upon as discussed above and disclose all of the claimed features as stated above except for the combined thermal and plasma oxidation process and where oxidation process comprises an oxidation environment with a N_2O flow rate between 500 and 5000 sccm at a chamber

pressure between 1 and 10 Torr, a wafer substrate temperature between 250 degrees C and 400 degree C, a plasma power between 250 Watts and 1000 Watts.

Narwankar et at. discloses a thermal and plasma oxidation process (See page. 6 paragraph [0080]). Narwankar et at. also discloses a method wherein the oxidation process further comprises: an oxidation environment with a N_20 flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr (See page. 6 paragraph [0080]); a wafer substrate temperature between 250 degrees C and 400 degree C (See page. 4 paragraph [0063]); a plasma power between 250 Watts and 1 000 Watts (See page. 5 paragraph [0063].

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the thermal and plasma oxidation process of Narwankar et at. in the oxidation of the tantalum nitride of Kim et at. and Stojalcovic et al. for it's known benefit as an oxidation process, oxidizing tantalum nitride layer to oxidized tantalum nitride. As both references are drawn to the oxidation process using thermal and plasma oxidation process a prima fade case of obviousness is established.

Regarding claims 13 and 18, Narwankar et al. discloses a method wherein the oxidation process further comprises: an oxidation environment with a N_20 flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr (See page. 6 paragraph [0080]); a wafer substrate temperature between 250 degrees C and 400 degree C (See page. 4 paragraph [0063]); a plasma power between 250 Watts and 1000 Watts (See page. 5 paragraph [0063]. According to Narwankar et at. These parameters can be adjusted, however, on the basis of empirical results. if required, to yield optimum results.

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the oxidation environment with a N_20 flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr and the wafer substrate temperature between 250 degrees C and 400 degree C and the plasma power between 250 Watts and 1000 Watts of Narwankar et at. in the oxidation of the tantalum nitride of Kim et at. and Stojakovic et at. for their known benefit as an oxidation process of tantalum nitride by thermal and plasma oxidation process.

The Invention, Generally

The invention is generally directed to Oxidized Tantalum Nitride as an Improved Hardmask in Dual-Damascene Processing in fabrication of semiconductor devices. A method of producing an oxidized tantalum nitride (TaO_xN_x) hardmask layer for use in dual-damascene processing is described. Fine-line dual-damascene processing places competing, conflicting demands on the hardmask. Whereas critical dimension control needs a thicker hardmask, optical lithographic alignment is frustrated by the opacity of thick tantalum nitride (TaN). The technique solves the problem of TaN hardmask opacity with increasing thickness by oxidizing the TaN layer. Oxidation of the TaN hardmask increases the thickness of the hardmask to two to four times its original thickness and simultaneously increases its transparency by greater than ten times. This

permits better CD control associated with a thicker hardmask while facilitating optical lithographic alignment.

The References, Generally

Kim et al. (US Pat. 2004/0214446) discloses nitrogen-free dielectric anti-reflective coating and hardmask. Methods are provided for depositing a dielectric material. The dielectric material may be used for an anti-reflective coating or as a hardmask. In one aspect, a method is provided for processing a substrate including introducing a processing gas comprising a silane-based compound and an oxygen and carbon containing compound to the processing chamber and reacting the processing gas to deposit a nitrogen-free dielectric material on the substrate. The dielectric material comprises silicon and oxygen. In another aspect, the dielectric material forms one or both layers in a dual layer anti-reflective coating.

Stojakovic et al. (US Pat. 2005/0051820) fabrication process for a magnetic tunnel junction device. A method of fabricating a magnetic tunnel junction (MTJ) device is provided. A patterned hard mask is oxidized to form a surface oxide thereon. An MTJ stack is etched in alignment with the patterned hard mask after the oxidizing of the patterned hard mask. Preferably, the MTJ stack etch recipe includes chlorine and oxygen. Etch selectivity between the hard mask and the MTJ stack is improved.

Narwankar et al. (US Pat. 2003/0025146) processes for making a barrier between a dielectric and a conductor and products produced therefrom. The formation of a barrier layer over a high k dielectric layer and deposition of a conducting layer over the barrier layer prevents intermigration between the species of the high k dielectric layer and the conducting layer and prevents oxygen scavenging of the high k dielectric layer. One example of a capacitor stack device provided includes a high k dielectric layer of Ta2O5, a barrier layer of TaON or TiON formed at least in part by a remote plasma process, and a top electrode of TiN. The processes may be conducted at about 300 to 700 C. and are thus useful for low thermal budget applications. Also provided are MIM capacitor constructions and methods in which an insulator layer is formed by remote plasma oxidation of a bottom electrode.

Comments Traversing the Rejection(s)

The independent claims are:

1. A method of forming an oxidized tantalum nitride hardmask for dual damascene processing
9. A dual damascene method of processing a semiconductor wafer
14. A dual-damascene method of processing a semiconductor wafer

In **claim 1**, a tantalum nitride layer is overlying the hardmask layers, and "subjecting the tantalum nitride layer to an oxidation process to convert said tantalum nitride layer to oxidized tantalum nitride (TaOxNx)."

In **claim 9**, there is etching before oxidation (see, e.g., left side of Fig. 2), and "subjecting the etched tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer."

In **claim 14**, oxidation occurs before etching (right side of Fig. 2), and "subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer; and lithographically etching the oxidized tantalum nitride layer to form trench openings therein."

Claims 1-5, 7-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Pat. 2004/0214446) in view of Stojakovic et al (US Pat. 2005/0051820).

Claims 6, 12, 13, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Pat. 2004/0214446) in view of Stojakovic et al (US Pat. 2005/0051820) further in view of Narwankar et at. (US Pat. 2003/0025146).

Kim is basically a simple damascene structure. Kim does have tantalum nitride, but only as a barrier layer (see 124, Fig. 2G). This does not suggest or disclose using TaN or TaON as a hardmask. Nor does it suggest the techniques of the present invention.

Kim recognizes the usefulness of a hardmask. see paragraphs 0082 and 0083

> [0083] A nitrogen-free dielectric hardmask layer 322 as described herein may then be deposited on the second dielectric layer 318 and patterned preferably using conventional photolithography processes to define the interconnect lines 320 as shown in FIG. 3B. The nitrogen-free dielectric hardmask layer 322 is a hardmask which may perform as a stop for chemical mechanical polishing techniques to allow removal of conductive material while protecting low k dielectric materials, such as the second dielectric layer 318, from damage during etching processes or from polishing processes, such as chemical-mechanical polishing. The hardmask layer 322 of the nitrogen-free dielectric material described herein has exhibited an etching selectivity of oxide or metal to hardmask of about 4:1 or greater, and in some instances has exhibited an etching selectivity of about 10:1 or greater of oxide or metal to hardmask.
>
> [0084] The nitrogen-free dielectric hardmask layer 322 is deposited as described herein. An example of a hardmask deposition includes supplying silane to a plasma processing chamber at a flow rate between about 100 sccm and about 700 sccm, supplying TEOS to

> the plasma processing chamber at a flow rate of about 2000 mgm or greater, supplying helium at a flow rate between about 500 sccm and about 10,000 sccm, maintaining a substrate temperature between about 250.degree. C. and about 450.degree. C., maintaining a chamber pressure between about 3 Torr and about 10 Torr, supplying an RF power of between about 100 watts and about 1000 watts for a 200 mm substrate, and spacing the substrate from the source of processing gas at a distance between about 300 mils and about 500 mils. The hardmask 322 is deposited at a deposition rate of about 2000 .ANG./min. The hardmask 322 was observed to have an etch selectivity of oxide or metal to hardmask of about 10:1.

But Kim's hardmask does not anticipate of render obvious the hardmask of the present invention.

Stojakovic mentions TaN and TaON, among others, that serve as a hardmask. For example,

> [0007] The problems and needs outlined above are addressed by embodiments of the present invention. In accordance with one aspect of the present invention, a method of fabricating a magnetic tunnel junction (MTJ) device is provided. This method includes the following steps. A patterned hard mask is oxidized to form a surface oxide thereon. An MTJ stack is etched in alignment with the patterned hard mask after the oxidizing of the patterned hard mask. **The hard mask may comprise one or more layers made from titanium, tantalum, tantalum nitride, titanium nitride, titanium oxide, tantalum oxide, or any combination thereof, for example.** As one example, the hard mask may include a tantalum nitride layer, a titanium layer over the tantalum nitride layer, and a titanium nitride layer over the titanium layer. The etching of the MTJ stack is preferably performed with an etch chemistry including oxygen and chlorine, and using a self-bias voltage between about -350 and about -380 volts, for example. (emphasis added)

However, Stojakovic doesn't mention the increase in film thickness - as a result of oxidation - as disclosed in the ***present invention***. For example,

> [0020] The present inventive technique employs oxidized tantalum nitride (TaN) as an improved hardmask for use in dual-damascene processing. By oxidizing a tantalum nitride hardmask (to produce TaOx Nx tantalum oxy-nitride), the thickness of the hardmask is increased by a factor of two to four times over unoxidized TaN, while simultaneously increasing the transparency of the hardmask by a factor of greater than ten times. The thicker TaOx Nx hardmask provides better critical dimension (CD) control against the etching processes used to etch hybrid or inorganic dielectrics. The increased transparency of the TaOx Nx hardmask permits accurate optical alignment of lithographic processes to underlying alignment features (typically formed in the base dielectric layer well below the hardmask layer).

The ***present invention*** discloses formation of TaONx hardmask for the purpose of pattern transfer. Stojakovic does not mention this - rather, it is mentioned – "A patterned hard mask is oxidized to form a surface oxide....." ([0007], quoted above)

Stojakovic mentions surface oxide. The present invention claims that TaN is oxidized through a

plasma to form a graded TaON film that increases in thickness 10 fold over the TaN Film. Both Kim and Stojakovic do not mention the gradation or thickness increase.

With regard to the ***present invention***, it is further important to note that "simply converting TaN to TaON" would not be a practical solution. A basic problem involved is that lithographic alignment through TaN rapidly decreases as TaN thickness increases. From this perspective, TaN should be thin. However, from a selectivity and CD control perspective, it is required that TaN be thick. As disclosed herein, the method to accomplish this is to oxidize the TaN which leads to an increase in the thickness of TaON.

Stojakovic states:

> [0011] In accordance with another aspect of the present invention, a method of fabricating a magnetic tunnel junction (MTJ) device is provided. This method includes the following steps. A hard mask is provided over an MTJ stack. The hard mask includes a titanium nitride layer over a titanium layer. A patterned photoresist layer is provided over the hard mask. The hard mask is etched through a majority of the titanium nitride layer with a first etch recipe. The hard mask is then etched through a remainder of the titanium nitride layer and a first portion of the titanium layer with a second etch recipe. The photoresist layer is then removed. The hard mask may further include a tantalum nitride layer, wherein the titanium layer is over the tantalum nitride layer. After removing the photoresist and ARC layers, the hard mask may be etched through the remainder of the titanium layer and at least a majority of the tantalum nitride cap layer with a third etch recipe. The hard mask may then be oxidized to form a surface oxide thereon.

The comments set forth hereinabove discuss why the present invention is different from both Kim and Stojakovic. To summarize, there are two methods of patterning the structure. The aim is to allow adequate lithographic alignment signal and simultaneously allow adequate etch selectivity window in concert with maintain critical dimensions during the subsequent etch processes. There are 2 ways to achieve this:

1. Use a thin TaN hardmask (<10nm). Apply ARC and photoresist. Lithographic alignment through the stack is easy as the metal is thin. After pattern transfer through the metal, oxidize the metal to increase the thickness of the metal to about 10 fold increase. The subsequent dual damascene etch will now have adequate hardmask protection to maintain good fidelity in CD.
2. Use a TaN hardmask (< 100nm). Oxidize the TaN to increase the thickness of the film by 10 fold. Now, lithographic align thro the TaON film and followup by pattern transfer through the TaON film.

A key feature of the ***present invention*** is that oxidizing the TaON results in an increase of the hardmask thickness that is not mentioned in Kim or Stojakovic.

Narwankar et al. (2003/0025146) is used in the rejection of dependent claims 6, 12, 13, 17 and 18. In Narwanker, it can be observed,

> [0063] The Ta2O5 dielectric film 14 may be deposited, for example by thermal CVD using a deposition gas mix comprising a source of tantalum, such as, but not limited to,

TAETO [Ta(OC2H5)5 and TAT-DMAE [Ta(OC2H5)4(OCHCH2N(CH3)2], and a source of oxygen such as O2 or N2O can be fed into a deposition chamber while the substrate is heated to a deposition temperature of between 300-500.degree. C. and the chamber maintained at a deposition pressure of between 0.5-10 Torr. The flow of deposition gas over the heated substrate results in thermal decomposition of the metal organic Ta-containing precursor and subsequent deposition of a tantalum pentoxide film. In one embodiment TAETO or TAT-DMAE is fed into the chamber at a rate of between 10-50 milligrams per minute while O2 or N2O is fed into the chamber at a rate of 0.3-1.0 SLM. TAETO and TAT-DMAE can be provided by direct liquid injection or vaporized with a bubbler prior to entering the deposition chamber. A carrier gas, such as N2, H2 and He, at a rate of between 0.5-2.0 SLM can be used to transport the vaporized TAETO or TAT-DMAE liquid into the deposition chamber. Deposition is continued until a dielectric film 14 of a desired thickness is formed. The desired thickness will vary depending upon the application that the capacitor is to be used for. For example, linear applications, such as for use in A/D conversion, generally uses a thickness of about 400-1000 .ANG., decoupling capacitors generally have a desired dielectric thickness of about 150-300 .ANG., and embedded DRAM applications generally have a desired thickness of about 80-150 .ANG.. Tantalum pentoxide (or tantalum oxide, as it is sometimes called) is a useful material in the production of memory capacitors because, with a k value of about 25, it provides a potential 4-to-6 fold increase in capacitance over silicon oxide, depending on the barrier material scheme that is used.

[0064] After deposition of the film 14, the film 14 is typically annealed to complete the oxygenation of the oxide layer. The film 14 can be annealed by any well known and suitable annealing process such a rapid thermal anneal or a furnace anneal in an ambient comprising an oxygen containing gas, such as O2 or N2 at a temperature between 800-850.degree. C., for example, for front end of the line processing. Back end of the line processing involves devices that have a lower thermal budget, and therefor the anneal is generally conducted at temperatures less than about 450.degree. C.

[0065] Alternatively, the film 14 can be annealed with highly reactive oxygen atoms generated by disassociating an oxygen containing gas, such as O2, with microwaves in a chamber which is remote or separate from the chamber in which the substrate is placed during the anneal. An anneal with reactive oxygen atoms which have been remotely generated is ideally suited for annealing a transition metal oxide dielectric film such as a tantalum pentoxide dielectric (Ta2O5). The annealing step balances the stoichiometry of the dielectric film 14 for optimal electrical properties because Ta2O5 deposits produce electrodes that are oxygen deficient and resistive (non-insulating). By annealing in oxygen, the correct stoichiometry is obtained.

[0066] Annealing of high-k films must be carefully controlled. The total thermal budget of a semiconductor device is limited. Exposure of the device to high-temperature anneals for extended periods can ruin the device. The annealing process can affect the substrate beneath the dielectric. For example, in Ta2O5 metal-insulator-silicon (MIS) structures for

DRAM applications, the bottom electrode consists of .about.20 .ANG. SiN on polycrystalline silicon. During annealing, oxygen diffuses through the Ta2O5 and reacts to form low-k SiO2 at the interface. As anneal process time increases, the capacitor stack storage capacity decreases. For e-DRAM applications, a typical treatment does not exceed about 30 minutes at a temperature of about 700.degree. C., although these parameters can vary with varying designs of devices to be treated and the thermal budgets which correspond to them.

Narwanker paragraphs 67-71 describe the chamber, as follows:

[0067] Prior to deposition of the top electrode 16, the dielectric layer 14 is next treated to form a boundary or barrier 18 on the surface of the dielectric layer 14 which will interface with the top electrode film 16. In one example treatment, a remote plasma nitridation (RPN) process is employed using N2 to form an extremely thin (about 5A) layer of TaON at the surface of the dielectric layer 14. In this process, the substrate, including the bottom electrode 12 and dielectric layer 14 are positioned in a process chamber for application of the barrier 18. FIG. 4 shows a chamber 20, which may be an anneal chamber, such as the Applied Materials XZ Anneal Chamber, for example, which may be used in carrying out the present invention. It is noted that the present invention is not limited by the chamber described with regard to FIG. 4, but may be carried out in other chambers, including other CVD systems used with the Endura system manufactured and sold by Applied Materials, Inc. of Santa Clara, Calif., RTP chambers used with the Centura mainframe of Applied Materials, and other chambers including those used in PVD, CVD, PECVD, RPECVD and RTPCVD processes.

[0068] Chamber 20 is a vacuum tight chamber, and may be made of aluminum, for example. A susceptor 22 is situated in the chamber 20. Susceptor 22 may also be made of aluminum or ceramic, and functions to support the substrate including the dielectric layer 14 during processing. The susceptor includes built in resistive heating, as is known in the art.

[0069] A vacuum pump system 24 is connected to the chamber 20 and produces and maintains the required vacuum conditions in the chamber for processing. A remote chamber 40, which may be water-cooled, is mounted to chamber 20, on top of chamber 20 in this example, although a side mount may also be possible. Chamber 40 is used to remotely excite or activate a corresponding process gas, e.g., by forming a plasma, prior to flowing the excited process gas into chamber 20 and over the dielectric layer 14 to react therewith. In the above mentioned example, chamber 40 receives a nitrogen containing gas, such as N2 or NH3 through a supply line 42 that is controlled by a pulse valve 44, or other valve mechanism suitable for this purpose. The pulse valve 44 may be a solenoid or piezoelectric valve. Additionally, an inert carrier gas, such as argon or helium may be inputted, which acts to prevent activated nitrogen from recombining. Chamber 40 supplies activated nitrogen species into chamber 20 through injection port 46, mounted through the lid of the chamber 20. Chamber 40 is used to generate a remote plasma with the inputted gas or gases, to activate the species before it is flowed into the chamber 20.

[0070] In the described embodiment, the chamber 40 is a microwave generated plasma chamber, such as one produced by ASTEX, of Wilmington, Mass., for example. Alternatively, any one of a number of other appropriate known devices for exciting gases remotely can be used. For example, inductively coupled plasma generation (e.g., RF plasma) may be used, wherein a chamber is wrapped with a coil through which current is passed. The gas to be excited is also inputted to the chamber as the current is being passed through the coil, which inductively generates a plasma by electromagnetically exciting the gas. Similarly, magnetically coupled plasma generation may be performed wherein electromagnets are used to electromagnetically couple to the gas to form a plasma.

[0071] A programmed controller 57 controls and coordinates the operation of chamber 40, vacuum pump 24, pulse valve 44 and heating of the susceptor 22 to achieve the operation which will now be described. A memory (not shown) within the controller 57 stores computer-readable instructions which cause the controller 57 to operate the system as described in the next section.

Narwanker paragraphs describe process parameters, as follows:

[0072] A substrate 10 having the dielectric layer 14 deposited thereon is fed into chamber 20 by a robot blade (not shown) through a slit valve (not shown) in the wall of chamber 20 under transfer pressure. Lift pins (not shown) may pass through lift pin holes (not shown) in the susceptor 22 to facilitate the transfer of substrates into and out of the chamber 20, as known in the art.

[0073] Once the substrate 10 is positioned on the susceptor 22 and the susceptor 22 is in the processing position, chamber 20 is then pumped down to about 1-2 Torr and the chamber 20 and substrate 10 are brought within a temperature range of about 300-425C. to ready the chamber for processing.

[0074] Next, a source gas containing nitrogen (e.g., N2 or NH3) is flowed into the chamber 40 through pulse valve 44 and converted to active nitrogen species by generating a plasma as described above, with microwave power being in the range of about 1400-4500 Watts. The activated nitrogen species are then flowed into chamber 20 through port 46 and allowed to pass over the surface of the dielectric layer 14, where it reacts with the Ta2O5 to form an extremely thin layer 18 of TaON (e.g., about 5 .ANG.). The activated nitrogen species are flowed into chamber 10 at a flow rate of about 0.5-2 slm. An argon or helium carrier gas may also be flowed with the activated species, at a rate of about 1-2 slm, to prevent recombination of the activated nitrogen species. The flow rates are such to maintain a pressure of about 1-2 Torr in the chamber 10 during processing, at a temperature of about 300-425C. These parameters can be adjusted, however, on the basis of empirical results, if required, to yield optimum results. It should be further noted, that the process temperature range is dependent upon the thermal budget of the device which is being treated. For example, for an e-DRAM, front end of the line application, a temperature range of about 600-700.degree. C. may be employed. In contrast, for back end

of the line capacitor devices, a temperature of about 300-350C. may be used at a pressure less than or equal to about 2 Torr. Typically, this processing is conducted for about 2 to 3 minutes, but this may also vary, and can be adjusted on the basis of empirical results to yield optimum results. The activated nitrogen may be used to nitridate other dielectric layers which require a barrier at an interface with a conducting layer, as noted above.

[0075] By moving the source of activated nitrogen to a remote plasma chamber, the chemistry can be controlled over a much broader range of operating and process conditions. For example, the temperature of the process can be run at about 300 C. to about 700 C., thereby helping to keep within the thermal budget. Typically maximum temperatures allowed for such processing should be kept below 750 C. so as not to damage the underlying logic gates. For MIM applications, the temperatures may be kept less than about 400 C. In addition, keeping the activation step separate from the deposition step insures that a very thin surface layer can be grown as the nitridated layer. That is, the nitrogen is not allowed to react within the dielectric layer, but only on the surface. That is, by separating the nitrogen plasma, the generation of activated nitrogen species above the substrate is prevented during the deposition of the dielectric layer. A wider range of process conditions are also available for conducting the deposition phase of the dielectric layer, due to the remote plasma generation.

[0076] Following the formation of the barrier 18, the top electrode 16 is next deposited, for example by a thermal CVD process. In this example, the top electrode is a film of TiN deposited by thermal CVD, although other materials, such as TaN or other metal, for example may be used for the top electrode. Any well known technology can be used to form the top electrode 16 including blanket depositing the conducting film over the barrier 18 and then using well known photolithography and etching techniques to pattern the electrode film and dielectric layer.

[0077] When depositing a TiN film using thermal CVD, NH3 and TiCl4 are typically used as components of the deposition gas, in which case NH3 and chlorine can react with Ta2O5 to reduce it, thereby scavenging oxygen from the dielectric layer. The TaON barrier 18 prevents this from occurring.

Narwanker paragraphs 78-79 similar to 72-77 except uses NH3

[0078] In another example of a process for forming a barrier 18, a thicker layer of TaON is formed on the surface of a Ta2O5 dielectric layer 14. Once the substrate is positioned on the susceptor and the susceptor 22 is in the processing position, the chamber 20 is then pumped down to processing pressure and brought to a processing temperature, as described above. In this example, NH3 is supplied to the remote plasma chamber 40 and a plasma is generated for an RPN process, using the same power range to generate the plasma as above.

[0079] The activated species (e.g., NH3,) is flowed into the chamber 20 through pulse valve 44 and port 46 and allowed to pass over the surface of the dielectric layer 14, where

it reacts with the Ta2O5 to form a thicker layer 18 of TaON (e.g., about 10-30 .ANG.) which has more oxygen vacancies than the TaON layer formed by activated N2. The source of nitrogen and the source of hydrogen need not be provided by NH3, but may be inputted to the chamber 40 separately in the form of N2 and H2, for example. Typically, this process is run for less than or equal to 2 minutes, although the time can be adjusted on the basis of empirical results to yield optimum results.

Narwanker paragraphs 80 describes RPO with 1-2 Torr

[0080] Following formation of the TaON layer by RPN, a mild oxidation process is performed by RPO to fully saturate any reduced TaO radicals that may exist in the layer. RPO is conducted by supplying O2 or N2O to the remote plasma chamber 40 and a plasma is generated for an RPO process. For example O2 gas may be supplied at about 2 slm to give an N2:O2 ratio of 1:2, at a pressure of about 1-2 Torr. For front end of the line applications, the processing temperature is about 500-600.degree. C., while for back end of the line applications, the processing temperature is about 300-400.degree. C., although these parameters can be adjusted on the basis of empirical results to yield optimum results. The foregoing process can also be used to nitridate other dielectric layers which require a barrier at an interface with a conducting layer, as noted above.

Narwanker paragraphs 86 describes RPO 1000-2000sccm, <2Torr, 300-400

[0086] FIG. 5 is a schematic sectional representation of a semiconductor stack of a type useful in making back end MIM capacitors. In this embodiment, a metal nitride bottom electrode layer 62 is first deposited. Next, the dielectric 64 of the construct is formed by remote plasma oxidation of the bottom electrode 62. The remote oxidation treatment may be conducted using any of the chambers previously discussed. Oxygen, in the form of O2, N2O, or other gas or gas mixture having a large amount of available oxygen is fed into a remote plasma chamber (such as remote plasma chamber 40, for example) and a plasma is generated for an RPO process. For example, O2 gas may be supplied at about 1-2 slm at a pressure of less than or equal to about 2 Torr. The annealing time for this RPO process is generally greater than 0 to about 5 minutes, more typically ranging from about 1 to 3 minutes, depending on the temperature used, although this time may be adjusted to vary the depth of oxygen penetration into the bottom electrode. For example, a higher temperature will generally require a shorter anncaling time. Since this construction is designed particularly for back end of the line processes, the processing temperature will generally run at around 300-400.degree. C. As in the previous examples, the processing parameters for this embodiment may also be varied on the basis of empirical results to yield optimum results.

A key element in Narwankar is that remote plasma is used. This is to obtain a defect free TaON dielectric. The ***present invention*** uses capacitive or inductively coupled direct plasma with a much higher flow range, higher pressure range and much lower plasma power. This aspect is not covered by Narwanker.

The "gist" of the ***present invention*** is essentially: The formation of TaON hardmask from

thermal-plasma oxidation that results in 10 fold increase in the film thickness. The increased thickness of the resulting film ensures good fidelity for litho alignment and CD control through etch.

Claim 1 discloses a method of forming an oxidized tantalum nitride hardmask for dual damascene processing including the steps of providing a semiconductor wafer with a tantalum nitride layer overlying the hardmask layers; and subjecting the tantalum nitride layer to an oxidation process to convert said tantalum nitride layer to oxidized tantalum nitride (TaOxNx). None of the prior art taken alone or in combination disclose providing a semiconductor wafer having one or more de layer overlying the hard mask layers and subjecting the tantalum nitride layer to an oxidation process to convert tantalum nitride layer to oxidized tantalum nitride (TaOxNx)." Accordingly, claim 1 should be allowable.

Claims 2-8 depend upon claim 1 and should also be allowable.

Independent claim 9 discloses "subjecting the etched tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer." For the same reasons given for the allowance of claim 1 claim 9 should be allowable.

Dependent claims 10 -14 depend upon claim 9 and should also be allowable.

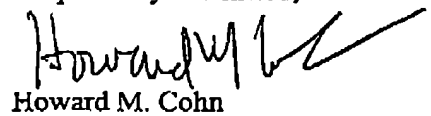
Claim 14 discloses providing a semiconductor wafer and forming a tantalum nitride layer over the second hardmask layer. The process also includes "subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer; and lithographically etching the oxidized tantalum nitride layer to form trench openings therein." This is not shown in the prior art taken alone or in combination and therefore claim 14 should be allowable.

Claims 15 -18 depend upon claim 14 and should also be allowable.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



Howard M. Cohn
Registration No. 25,808

Howard M. Cohn
21625 Chagrin Blvd. Suite 220
Cleveland, OH 44122
Voice (216) 752-0955